A CMOS neuroelectronic interface based on two-dimensional transistor arrays with monolithically-integrated circuitry

C.H. Chang [a,1], S.R. Chang [a,1], J.S. Lin [a,1], Y.T. Lee [b], S.R. Yeh [b], H. Chen [a,*]

[a] Institute of Electronics Engineering, National Tsing Hua University, 30013 HsinChu, Taiwan
[b] Institute of Molecular Medicine, National Tsing Hua University, 30013 HsinChu, Taiwan

ARTICLE INFO

ABSTRACT

The ability to monitor and to elicit neural activity with a high spatiotemporal resolution has grown essential for studying the functionality of neuronal networks. Although a variety of microelectrode arrays (MEAs) has been proposed, very few MEAs are integrated with signal-processing circuitry. As a result, the maximum number of electrodes is limited by routing complexity, and the signal-to-noise ratio is degraded by parasitics and noise interference. This paper presents a single-chip neuroelectronic interface integrating oxide-semiconductor field-effect transistors (OSFETs) with signal-processing circuitry. After the chip was fabricated with the standard complementary-metal-oxide-semiconductor (CMOS) process, polygates of specific transistors were etched at die-level to form OSFETs, while metal layers were retained to connect the OSFETs into two-dimensional arrays. The complete removal of polygates was confirmed by high-resolution image scanners, and the reliability of OSFETs was examined by measuring their electrical characteristics. Through a gate oxide of only 7 nm thick, each OSFET can record and stimulate neural activity extracellularly by capacitive coupling. The capability of the full chip in neural recording and stimulation was further experimented using the well-characterised escape circuit of the crayfish. Experimental results indicate that the OSFET-based neuroelectronic interface can be used to study neuronal networks as faithfully as conventional electrophysiological tools. Moreover, the proposed simple, die-level fabrication process of the OSFETs underpins the development of various field-effect biosensors on a large scale with on-chip circuitry.

© 2008 Elsevier B.V. All rights reserved.

1. Introduction

Many studies indicate that neurons employ changes of trans-membrane potential to communicate with each other, and information is encoded as ensembles of neural activity (Zigmond et al., 1999). To unveil how neurons can form a variety of functional networks, the ability to monitor and to elicit neural activity with a high spatiotemporal resolution is essential. However, conventional tools like glass pipettes are limited by their sizes, making it difficult to build a neuroelectronic interface with more than ten channels.

The rapidly-growing microelectronic technology has shed light on this obstacle, facilitating the fabrication of high-density microelectrode arrays (MEAs) with customised geometry (Rutten, 2002; He, 2005; Olsson and Wise, 2005; Patolsky et al., 2006). The in-plane MEAs are particularly useful for building a noninvasive, multi-site interface with neural tissues (Eversmann et al., 2003; Lambacher et al., 2004; Heer et al., 2006, 2007; Meyburg et al., 2006; Claverol-Tinture et al., 2007; Giovangrandi et al., 2006). Such an interface enables the long-term study of neural development and plasticity (Breckenridge et al., 1995; Jimbo et al., 2003; Morin et al., 2005; Vato et al., 2003). Most MEAs interface with neurons extracellularly. With microelectrodes located intimately near a neuron, neural activity is monitored or elicited by capacitive coupling. The coupling efficacy depends very much on the impedance across the neural membrane, the electrode impedance, and the proximity (sealing) of the electrodes to the neuron (Eversmann et al., 2003; Vassanelli and Fromherz, 1998; Castellarnau et al., 1995). Limited by the maximum level of sealing, extracellular recording is only adequate for detecting action potentials (APs), but not post-synaptic potentials which are important for the study of neural plasticity. To record postsynaptic potentials and to improve sensitivity, intracellular recording by patch-clamping neurons with micro-holes was proposed (Klemic et al., 2002). However, the intracellular approach unavoidably damages neuronal membranes, leading to neuronal death within several hours. In addition, the diameter of micro-holes is greater than 1 μm, making it difficult to achieve a sealing as satisfactorily as does a conventional

micropipette with a diameter of around 200 nm. Extracellular MEAs are thus more favourable for interfacing with neurons for more than one month.

However, MEAs are seldom integrated with signal-processing circuits, without which the maximum number of electrodes is limited by the compromise with routing complexity, and the signal-to-noise ratio is degraded by parasitics and noise interference (Jenkner et al., 2001; Parak et al., 1999; Hutzler and Fromherz, 2004). The difficulty in integration is attributed to the fact that micromachining processes for modifying electrode surfaces, or for creating customized geometry, are not fully compatible with the standard CMOS technology, the main technology for fabricating integrated circuits. For example, coating inert metals (Pt or Ir) on electrode surfaces is essential for avoiding the erosion of electrodes (He, 2005), while gaining access to deposit inert metals in a standard CMOS technology can be costly and even hindered when equipment contamination is concerned. Electrode modification is thus normally carried out upon the completion of the standard CMOS process. However, post-CMOS micromachining processes are particularly constrained for IC designers who adopt a multiple-project-wafer approach and hence receive dies instead of a full wafer. The limited die size makes it difficult to carry out processes even as trivial as coating photoresist for photolithography.

Under the aforementioned concerns, neuroelectronic interfaces based on the oxide-semiconductor field-effect transistors (OSFET) become attractive (Fromherz and Offenhausser, 1990; Hutzler and Fromherz, 2004), because the recording relies on purely capacitive coupling through the gate oxide of transistors. Long-term usage is thus achieved without the need for electrode modification. However, the gate-removal process proposed by Fromherz et al. sacrifices all metal layers, impeding the connection of transistors into a two-dimensional array, not to mention the integration with signal-processing circuitry. This constraint compelled Eversmann et al. to integrate Pt-coated electrodes with CMOS technology, so as to image neural activity at a high spatial resolution (Eversmann et al., 2003; Lambacher et al., 2004). Heer et al. further demonstrated a single-chip system integrating Pt electrodes with both recording and stimulating functions (Heer et al., 2006). The integration with cell-immobilising structure has also been reported (Greve et al., 2007). Nevertheless, micromachining process for coating Pt is costly, as discussed above. Berdondini et al. thus adopted a chemical approach to deposit gold on electrodes of a CMOS chip at die-level (Berdondini et al., 2005).

Instead of employing metal electrodes, this paper proposes a CMOS-compatible, neuroelectronic interface based on two-dimensional arrays of OSFETs. The OSFETs can be fabricated by a simple, die-level micromachining process. Fig. 1 illustrates the cross-sectional view of the structure of the OSFET. The OSFET has a circular active (sensing) region whose diameter is designed to be smaller than the size of a neuron. The OSFET exhibits three major differences from that proposed by Fromherz et al. First, only materials on top of the active region of the OSFET are removed, while metal layers are retained for interconnection. Secondly, a multifinger structure is employed to increase the transconductance significantly. Thirdly, the field oxide around the active region forms a circular hole of 7 μm deep, which could enhance the immobilisation of neurons cultured on top of the active region (Zeck and Fromherz, 2001). Moreover, the OSFET is fabricated from P-type transistors in the N-well. Through a gate oxide of only 7 nm thick, each OSFET is able to not only record but also stimulate neural activity by applying voltage pulses to the N-well, as illustrated by Fig. 1.

A CMOS chip comprising two-dimensional OSFET arrays, multiplexers, and recording amplifiers has been realised with the TSMC 0.35 μm CMOS technology. After die-level, post-CMOS process,

the reliability of the OSFETs was carefully examined by scanning their structures with high-resolution microscopes, as well as by measuring their current–voltage characteristics. The recording and stimulating functions of the full chip were further experimented using the well-characterised escape circuit of the crayfish, *Procambarus clarkia* (Furshpan and Potter, 1959; Watanabe and Grundfest, 1961; Tsai et al., 2005). By comparing with conventional electrophysiological tools, the capability of the OSFET chip and its future improvements are discussed and concluded.

2. Methods

2.1. Fabrication of the multifinger OSFET

Fig. 1 illustrates the post-CMOS process for fabricating the multifinger OSFET. As coating photoresist over a die evenly is difficult, stacks of metal layers are utilised to define the active region of an OSFET. In the passivation layer, the passivation above the active region is opened, while that above the wire-bonding pads is retained. Once the chip was fabricated with the standard CMOS process, metal layers were removed by wet etching with "piranha"(H_2SO_4:H_2O = 2:1) at 85 °C for 80 min. The multifinger polygates were then removed by wet etching with diluted KOH (KOH:DI water = 1:2 by weight) at 80 °C for 20 s. Subsequently, the passivation on wire-bonding pads was opened by reactive-ion etching. By placing the pads around the periphery of the chip, a simple mask such as fragments of a silicon wafer was sufficient for protecting the OSFETs and the circuitry during the reactive-ion etching. As a result, the die-level micromachining process avoided photolithography and preserves metal layers for interconnection.

The circular active region of the OSFET is designed to have a diameter of 12 μm, smaller than the size of cultured neurons such as the hippocampal neurons of rats (20 μm). This design allows the active region to be covered entirely by the cell body of a neuron, so as to guarantee good selectivity. Inside the active region, the OSFET has five polygates with an effective W/L of 50 μm/1 μm. The minimum linewidth (0.35 μm) is not applied in order to facilitate the complete removal of polygates.

2.2. Monolithically-integrated circuitry

Fig. 1 also shows the full circuit integrated with individual OSFETs. The multiplexers enable each OSFET to be addressable for either recording or stimulation. For neural recording, a current amplifier similar to that proposed in Fromherz and Offenhausser (1990) and Eversmann et al. (2003) is employed. Transistor M2 sets the biasing current and thus the transconductance of the OSFET. With biasing current varying from 1 to 256 μA, the transconductance can vary from 50 to 800 μA/V. As neural activity is transduced into changes in the drain current of the OSFET, the current I_d becomes nonzero and I_d is amplified by 25 times with OPA1 and M3–M6. The amplified current is then fed into the current–voltage converter whose feedback resistance is tunable between 30 and 100 k (Banu and Tsividis, 1982). Together with the OSFET's adjustable transconductance, the overall gain of the recording circuit can vary from 40 to 2000 V/V, facilitating the recording of neural activity across several orders of magnitude.

For neural stimulation, a 16-to-1 multiplexer is used to select the N-well of one OSFET for applying stimulating signals. To prevent the PN junction between the source/drain and the N-well from being forward biased, the source is disconnected from V_S and the drain voltage is set by V_{ref1} through the virtual short provided by OPA1. Based on the point-contact model (Weis and Fromherz, 1997; Fromherz et al., 1993), the recording and stimulating capability of
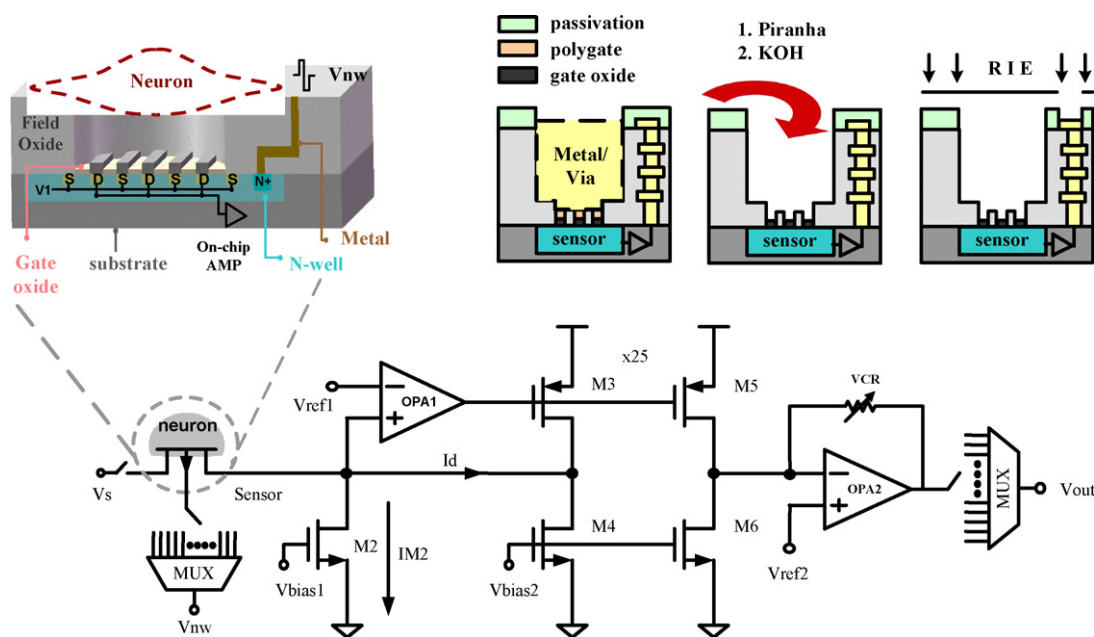
Fig. 1. The structure of the multifinger OSFET and its full circuit integrated on the same chip. The die-level micromachining process for fabricating the OSFET is illustrated at the top-right corner.

the full circuit has been estimated analytically and simulated with the HSPICE (Lin et al., 2007).

2.3. System description

Fig. 2 shows the microphotograph of the CMOS chip containing one 8×3 multifinger OSFET array, one 4×4 rectangular OSFET array, multiplexers, and recording amplifiers. The chip size is 2.7×2.5 mm^2, and the maximum power consumption of each recording circuit is 1.14 mW. The rectangular OSFETs having large rectangular active regions (20×20 μm^2, 30×30 μm^2, 40×40 μm^2, and 50×50 μm^2) were mainly implemented for monitoring the progress of the micromachining process. Therefore, the rectangular OSFETs were not connected with recording amplifiers, but their N-wells were accessible for neural stimulation. The separation between any two OSFETs was designed to be 40 μm, preventing a single neuron from covering more than two OSFETs. A testing circuit with the OSFET's polygate retained was also included to characterise the effect of micromachining process on the circuitry (Lin et al., 2007). Moreover, multifinger OSFETs with their sources and drains connected to probe pads were included as testkeys for electrical characterisation of the post-processed OSFETs and for the modeling of the neuron-OSFET interface (Weis and Fromherz, 1997). After micromachining processes, the chip was wire-bonded to a printed-circuit board (PCB), to which a glass O-ring was attached to form a culturing bath, as shown in Fig. 2. The entire chip surface except for the OSFET area was then coated with industrial epoxy (WK-8126H, WinKing) to prevent short circuits introduced by neural buffers in the bath.

2.4. Biological experiments

The chip's capability in neural recording and stimulation was experimented using the well-characterised escape circuit of the crayfish. The diagram at the top-left corner of Fig. 2 illustrates the functionality of the escape circuit. The lateral giant (LG) neurons (LG6) receive inputs from the mechanosensory afferents (SA) in the tail. Once the afferents are stimulated simultaneously by the

approach of a predator, LG6 neurons generate action potentials and propagate the APs to posterior LG neurons (LG5 and LG4) through electrical synapses. The sequential firings of LG neurons subsequently induce muscle contraction for the crayfish to escape from the predator.

Fig. 2 also shows the experimental setup. The nerve fiber of the crayfish, dissected less than 30 min before each experiment, was placed in the culturing bath with crayfish saline (210 mM NaCl; 15 mM CaCl$_2$, 5.4 mM KCl, 2.6 mM MgCl$_2$ and 5 mM HEPES, pH 7.4). One twisted, teflon-coated silver wire (no. 1) was placed in close proximity to the sensory afferents for stimulating the SAs extracellularly, while the other silver wire (no. 2) was used to record extracellularly the activity of the LG neurons located above the OSFET arrays. The signals recorded by the silver wire (no. 2) provided a credible reference for comparison with the signals recorded by the OSFET arrays. To enhance the sealing between the OSFET arrays and the crayfish nerve, the nerve fiber was pressed against the OSFET arrays by a micromanipulator (no. 3). Finally, the Ag/AgCl wire (no. 4) set the bias voltage in crayfish saline. Signals recorded by the silver wire (no. 2) were amplified with a commercial AC amplifier (A-M Systems 1700, USA). Recordings of both the silver wire and the OSFET chip were then low-pass filtered at 10 kHz, digitised through the PCI-1602 data-acquisition card (ICP DAS,Taiwan), and analysed with a graphical-user-interface application designed by the National Tsing Hua University, Taiwan.

3. Results and discussion

3.1. Gate-removal process

A post-processed OSFET was cut into half by the Focus-Ion-Beam system. The cross-section of the OSFET was then photographed by the scanning-electron-microscope (SEM), as shown in Fig. 3. The two subfigures at the bottom-right corners illustrate the top views of the OSFETs before and after the gate-removal process. The subfigure on the right, in contrast to that on the left, reveals clearly that the metal reflection disappeared after the gate-removal process. This result not only indicates the removal of metal layers, but also
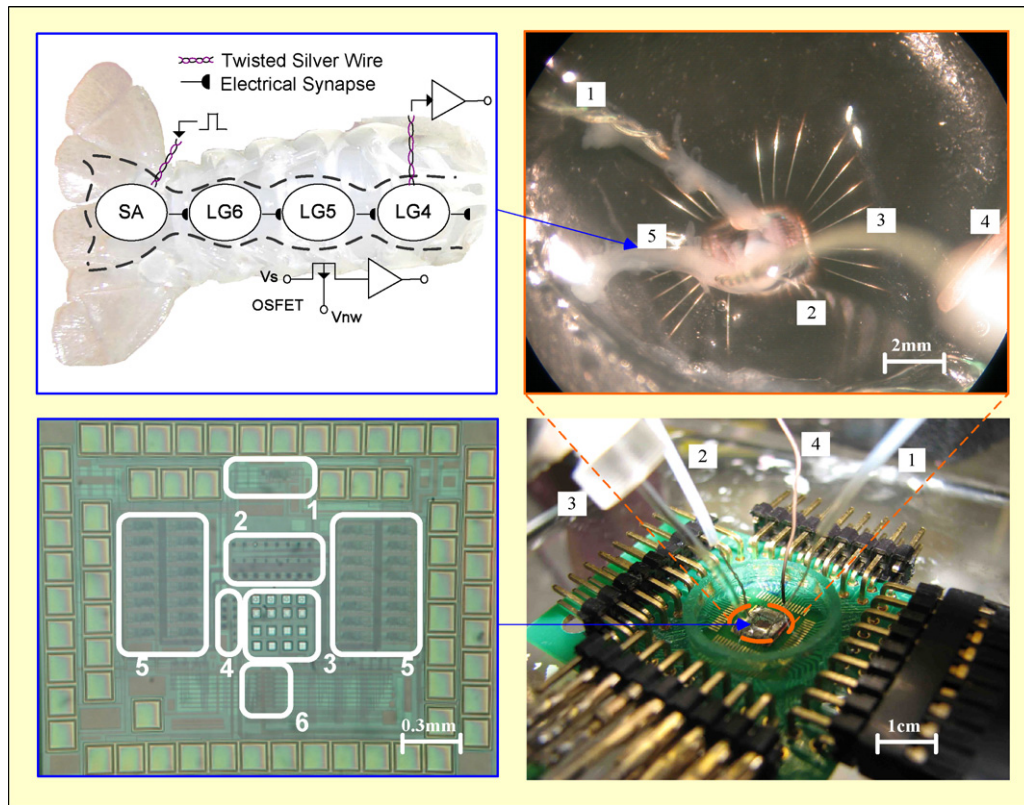
Fig. 2. The packaged OSFET chip and its setup for biological experiments. The microphotograph at the bottom-left corner shows that the chip contains (1) testing circuit, (2) one 8×3 multifinger OSFET array, (3) one 4×4 rectangular OSFET array, (4) multifinger OSFET testkeys, (5) recording amplifiers, and (6) multiplexers. The diagram at the top-left corner illustrates the escape circuit of the crayfish. The experimental setup contains (1) a silver twisted wire for stimulating sensory afferents, (2) a twisted silver wire for recording lateral giant neurons (3) a micromanipulator, (4) an Ag/AgCl reference electrode, and (5) dissected nerve fiber of the crayfish.
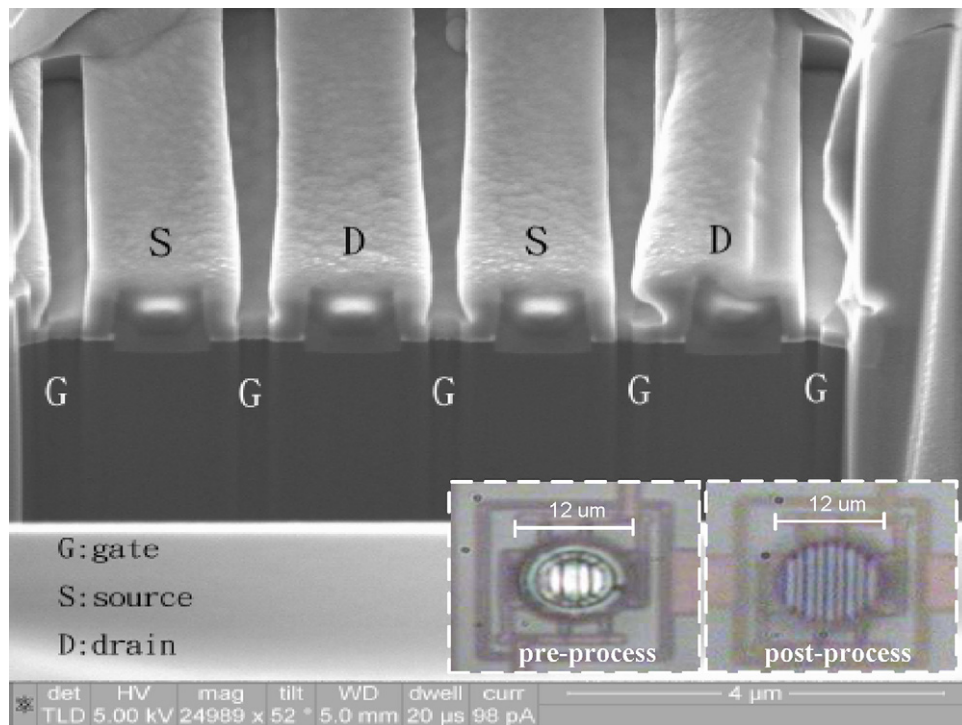

Fig. 3. The SEM photograph of a multifinger OSFET after the application of the post-CMOS process. The images at the bottom-right corners are the top views of the pre-processed and post-processed OSFETs.

relieves the concern that the impurity accumulated between metal layers could had impeded metal etching. The surface profile of one row of rectangular OSFETs was further scanned by an α-stepper. The active regions of OSFETs had a depth of around 7 μm (data not shown), agreeing with the technology profile provided by the TSMC. The complete removal of metal layers was thus confirmed. Furthermore, the SEM photo in Fig. 3 reveals that the OSFET exhibited five rectangular grooves after the etching of polygates, indicating the removal of polygates clearly.

3.2. Electrical test

To examine whether the OSFETs and the circuitry were affected by micromachining process or by the contact with neural saline, the electrical characteristics of the chip were first tested with the crayfish saline filled in the bath, wherein an Ag/AgCl electrode was immersed to set or to record the saline potential.

The yield of the OSFETs was first investigated by measuring the current–voltage (I–V) relationship of 30 OSFET testkeys. With the saline potential set to 0 V and the source voltage of OSFETs swept from 0 to 3 V, 27 out of the 30 OSFETs exhibited normal I–V curves. The proposed post-CMOS process thus produced a yield of 90%. One major concern was whether the thin gate oxide was well retained and was able to resist moisture or ion diffusion from the saline (Morrison et al., 1980). To investigate this issue, the I–V curves of the same OSFET were measured in four days. All curves except for the original one overlap with each other (see Supplementary). The original curve was measured immediately after the filling of saline, at which instance the ion concentration in the active region might have yet to reach its equilibrium. In addition, ion diffusion into the gate oxide introduced extra sensory drifts, which normally settled at a constant value within several hours (Morrison et al., 1980). The curves measured after 24 h (Day1–Day4) thus had negligible differences. Similar results were obtained from all OSFETs, indicating that the OSFET was robust against the exposure to the saline.

To examine the process variation across OSFETs, the I–V curves of 12 OSFET testkeys distributed on four different dies were measured. All the testkeys had an identical size and each three were on the same die. As having the same gain across an OSFET array is important for neural recording, the relationship between the transconductance (g_m) and the biasing current (I_s) was derived from the I–V curve of each OSFET. Fig. 4 plots the g_m–I_s curves of OSFETs on different dies, as well as that of three pre-processed testkeys on a single die. Each curve is averaged over three OSFETs on the same die, with the error bars indicating standard deviations calculated at various I_s. The variation across different dies is apparently greater than that specified by the foundry, implying the post-CMOS process has introduced extra variations. Nevertheless, the variation across different OSFETs on the same die is not significantly larger that across pre-processed testkeys (the curve UC). Therefore, the post-CMOS process mainly introduced variation across different dies, and the variation within the same die should be able to be compensated by the calibration circuit proposed in Eversmann et al. (2003). More interestingly, Fig. 4 reveals that all post-processed OSFETs have smaller transconductance than the pre-processed OSFETs. The transconductance of a transistor in saturation region is given by

$$g_m = \sqrt{2\mu Cox(W/L)I_D} \tag{1}$$

where μ, Cox, W/L and I_D denote the carrier mobility, gate-oxide capacitance, size, and drain current of the transistor, respectively. Given that pre-processed and post-processed OSFETs had identical size and biasing current, the reduction in transconductance should be attributed to the decrease in Cox. Cox could become smaller if
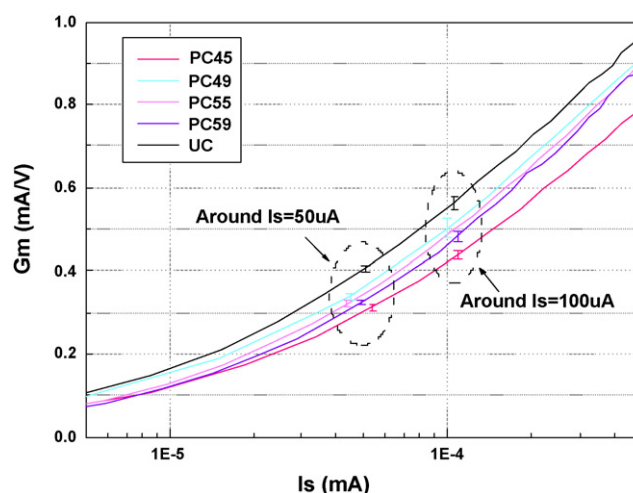

Fig. 4. The curves of transconductance versus biasing current for 12 post-processed OSFET testkeys on four different dies, as well as for three pre-processed testkeys on a single die. Each curve is the average over three testkeys ($n = 3$) on the same die and the error bars correspond to standard deviations (S.D.s) calculated at various bias current ($I_s = 50\,\mu A$ and $I_s = 100\,\mu A$). The S.D.s of the pre-processed testkeys (UC) are 6.13 μA/V and 15 μA/V for $I_s = 50\,\mu A$ and 100 μA, respectively. The S.D.s of the four processed chips are 8.67 μA/V and 12.5 μA/V for PC45, 5.41 μA/V and 25 μA/V for PC49, 8.39 μA/V and 1.21 μA/V for PC55, 6.16 μA/V and 11.5 μA/V for PC59.

the polygate above the gate oxide was not removed completely and oxidised into silicon dioxide, leading to an effectively thicker oxide layer. This also explains why the micromachining process mainly introduces variation across different dies, as the extent of polygate removal can easily vary from one die to another.

The recording functionality of the full circuit had been examined by applying sinusoidal signals into the buffer (Lin et al., 2007). The OSFET chip was able to record sinusoidal signals with an amplitude of more than 1 mV, while the recorded signal could hardly be distinguished from the noise as the amplitude reduced to 400 μV. As the gain of the recording circuit was 400, the output noise measured in the absence of the sinusoidal signal was 17 mV$_{RMS}$, corresponding to an input-referred noise of 42.5 μV$_{RMS}$. This noise level is slightly unsatisfactory because extracellular neural signals can be as small as 20 μV (He, 2005). The noise spectra of pre-processed and post-processed OSFET testkey were further measured and compared (see Supplementary). The post-processed OSFET appeared to exhibit extra noise, especially for the frequency above 1 kHz. While micromachining process may introduce extra noise by inducing more trapping states in the gate oxide, the significant increase in high-frequency noise implies there are other types of noise, e.g. random ion flows above the gate oxide. To take full advantage of increasing transconductance with the multifinger structure, the noise level must be reduced. The main causes of noise and possible improvements will thus be discussed in Section 3.5. The stimulation function had also been tested by applying a 3-V pulse to the N-well of one multifinger OSFET (Lin et al., 2007). The induced potential change in the saline was more than 200 mV. Given a good sealing between the OSFET and the neuron cultured on top, the potential change was sufficient for eliciting neural activity.

3.3. Recording from the escape circuit of the crayfish

In the setup shown in Fig. 2, a monophasic pulse with a pulse-width of 0.2 ms was applied to the silver wire (no. 1) to stimulate the sensory afferents. Simultaneous activation of the afferents subsequently induced action potentials in the LG neurons. Pilot experiments showed that the OSFET chip was able to record the

neural activity extracellularly and amplified it into several hundreds of milli-volts. To validate the recording of the OSFET chip, both the OSFET chip and another silver wire (no. 2) were used to record the same event, and their recordings were acquired and compared by the same data-acquisition system. Fig. 5 shows the recordings obtained as the sensory afferents received different levels of stimulation. According to the recordings of the silver wire (the upper graph in Fig. 5), LG neurons were activated about 1 ms after the stimulation, and the response time decreased with the pulse amplitude. As the pulse amplitude reduced to 1.4 V, no action potential was recorded. Therefore, a pulse amplitude greater than 1.5 V was required for exciting the sensory afferents and thus the LG neurons. The recordings of the OSFET chip (the lower graph in Fig. 5) revealed exactly the same phenomena. With the on-chip recording amplifier, the amplitude of the recordings was several hundred times greater than that acquired by the silver wire. The detected spikes were less obvious because the sealing between the OSFET and the nerve floating in the saline was not easily maintained in a good condition consistently. In addition, the spike shapes differed from those detected by the silver wire not only because the OSFET recorded LG neurons in a different ganglion (LG5 in Fig. 2), but also because extracellular recordings depended very much on the type and the direction of ion flows around OSFETs (Fromherz, 1999; Vassanelli and Fromherz, 1998). Compared to the recordings of the silver wire, the activity recorded by the OSFET chip preceded that by the silver wire by 0.3 ms consistently. The timing difference coincided with the time required for transmitting an action potential from one LG ganglion to its posterior ganglion (Watanabe and Grundfest, 1961). Therefore, the timing difference was simply attributed to the fact that the LG neurons (LG5 in Fig. 2) above the OSFET were closer to the sensory afferents than the LG neurons (LG4) in proximity to the silver wire. These promising results demonstrate that the OSFET chip can record neural activity as faithfully as conventional tools.

3.4. Stimulating the LG neurons

The LG neurons can also be excited directly by extracellular voltage pulses. But experiments revealed that a single multifinger OSFET could not stimulate LG neurons effectively, mainly owing to the poor sealing between the OSFET and the LG neurons. Instead, LG neurons were successfully stimulated by applying voltage pulses to the common N-well of six OSFET testkeys. Fig. 6 shows the activity of LG neurons recorded by the silver wire (no. 2). A stimulating pulse of 5 V at 1 kHz induced periodic activity with a consistent lag of
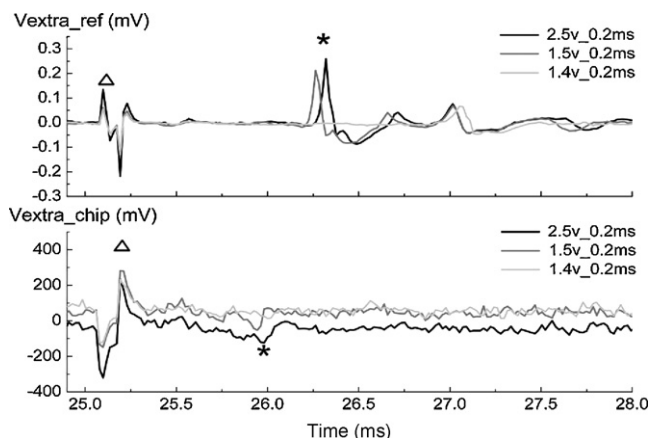

Fig. 5. Extracellular recording of LG neurons obtained by the silver wire (the upper graph) and the OSFET chip simultaneously (the lower graph) as different levels of voltage pulses were applied to sensory afferents. In all plots, the triangles denote stimulation artifacts and asterisks the neural activity.
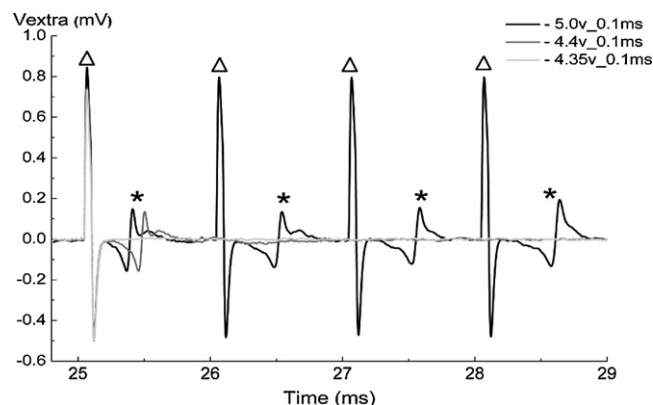

Fig. 6. The activity of LG neurons elicited by the OSFET testkeys as different levels of voltage pulses were applied to the N-well of the testkeys. The triangles denote stimulation artifacts, and asterisks the neural activity.

400 ms. The lag increased slightly as the pulse amplitude decreased to 4.4 V, and the neural activity diminished when the amplitude became 4.35 V. The absence of neural activity in the last case proved that the periodic activity was elicited by the OSFET, instead of being spontaneous firings. Moreover, the minimum amplitude required for inducing neural activity was 4.4 V in this experiment.[2]

In addition to a good sealing, inducing sufficiently large current density close to a neuronal membrane is crucial for stimulating neurons extracellularly. The current density depends on two factors for the OSFET chip. One is the sealing between the OSFET and the neuron, and the other is the coupling capacitance provided by the OSFET. The minimum current required for stimulating LG neurons, as well as the current induced by a single OSFET, was thus further measured (detailed in the Supplementary). First of all, the surface of the nerve fiber was sucked tightly by a glass pipette to provide a good and unique sealing at its tip. An Ag/AgCl electrode in the pipette was then connected to the reference ground. A pure silver wire except for its tip was coated with epoxy (AB gel) and used to generate capacitive stimulation as an OSFET. With voltage pulses applied either to the OSFET or to the silver wire, currents were induced to flow through the Ag/AgCl electrode and the glass pipette. A large enough current subsequently elicited neural activity at the tip of the suction pipette where the unique sealing was created. Experiment with the silver wire revealed that a single 4.8-V pulse with a duration of 0.1 ms was sufficient for inducing neural activity similar to that shown in Fig. 5. The corresponding stimulating current was 100 μA. However, a single OSFET induced only 6 μA with a 5-V pulse (detailed in the Supplementary). To stimulate LG neurons with a single OSFET, the area of the active region has to be increased.

4. Discussion

This study demonstrates the feasibility of fabricating two-dimensional OSFET arrays with simple, die-level, post-CMOS process. The yield of the proposed process is 90%, and the process variation across OSFETs on the same die remains comparably small. As the gain for neural recording depends on the transconductance of an OSFET, the process variation can be largely calibrated by the circuits proposed in Eversmann et al. (2003). Therefore, the CMOS-compatible OSFETs proposed in this study not only avoid the need for coating inert metal on electrodes (Eversmann et al., 2003;

---

[2] It is notable that the minimum amplitude varies from one trial to another, depending very much on the proximity to the neurons and neural health.

Lambacher et al., 2004; Heer et al., 2006), but also eliminate the routing limitation faced by previously-proposed OSFETs (Fromherz and Offenhausser, 1990; Hutzler and Fromherz, 2004). The capability of the OSFET chip in neural recording and stimulation has also been demonstrated, while several aspects have yet to be improved before the OSFET neuroelectronic interface is applicable to general neuroscience research.

The transconductance of OSFETs was found reduced after the post-CMOS process, implying that polygates might not be removed completely. However, the thin gate oxide can be easily damaged by over-etching, as shown by Fig. 3. To identify the optimum length of time for etching polygates completely, it is crucial to incorporate testkeys like two pads connected by a polygate wire. The optimum etching time can then be identified by detecting the exact instance at which the two pads become open-circuit.

For neural recording, the minimum detectable signal is 400 μV, mainly limited by the noise level of the system. The noise level is comparable to that reported in Lambacher et al. (2004) ($280 \mu V_{RMS}$) but greater than that achieved by conventional tools or the microelectrodes in Heer et al. (2006, 2007) ($11.7 \mu V_{RMS}$). The main difference between these works is that neural activity is transduced and amplified as current signals in our work and in Lambacher et al. (2004), but as voltage signals in Heer et al. (2006, 2007). As it is not easy to filter current-mode signals in integrated circuits, the lack of on-chip filters leads to less satisfactory noise performance. According to the circuit shown in Fig. 1, the total output noise, e_{tot}, is given by

$$e_{tot} = R_f \times (25 \times (e_{n,OSFET}^2 g_{m,OSFET}^2 + e_{n2}^2 g_{m2}^2 + (e_{n3}^2 + e_{n,OPA1}^2)g_{m3}^2$$
$$+ e_{n4}^2 g_{m4}^2) + e_{n5}^2 g_{m5}^2 + e_{n6}^2 g_{m6}^2) + e_{n,OPA2}^2 \qquad (2)$$

where e_{ni} and g_{mi} denote the noise and the transconductance of the transistor Mi, respectively. $e_{n,OPA1}$ and $e_{n,OPA2}$ are noise outputs of OPA1 and OPA2, respectively, and R_f the feedback resistance of OPA2. As the transconductance of the OSFET ($g_{m,OSFET}$) is much greater than others, Eq. (2) indicates that noise in the OSFET has the largest gain and thus dominates e_{tot}. Moreover, noise in the OSFET was found to increase remarkably after the post-CMOS process. The noise should thus be reduced or avoided as much as possible.

Except for the intrinsic noise relating to trap states at the oxide-semiconductor interface, the OSFET should exhibit at least three extra noise sources. The first is the disturbance of ion flows above the gate oxide. The second is the interference coupled to the source node of the OSFET (V_S in Fig. 1), which receives the same gain as neural signals. Finally, the light penetrating through the gate oxide also introduces non-negligible noise currents. Given so many noise sources in OSFETs, it is essential to convert the current signal of the OSFETs back to a voltage signal at the front end as early as possible and to filter the signal in voltage mode before amplification. On the other hand, the interference at the source node could be greatly reduced by employing an "OSFET differential pair", composed of two identical OSFETs with only one having its gate removed. The interference would thus become a common-mode signal and be rejected directly. Finally, the floating-gate structure can be adopted to reduce the light-induced currents (Cohen et al., 2004; Meyburg et al., 2007), but the signal level will be compromised due to the separation between sensing and active regions.

For neural stimulation, the coupling capacitance provided by a single OSFET was found insufficient for stimulating LG neurons. Although the constraint can be relieved by increasing the size of the OSFET, increasing the size will degrade the selectivity of neural recording. As cultured neurons are expected to have a better sealing with the OSFET, it is important to further identify the minimum size required for stimulating cultured neurons. This result will indicate whether using separate OSFETs for neural recording and stimulation is necessary (Hutzler and Fromherz, 2004; Zeck and Fromherz, 2001).

Finally, in addition to functioning as a neuroelectronic interface, the CMOS-compatible OSFETs proposed here are able to be transformed into various field-effect biosensors with on-chip circuitry for a wide range of applications (Bergveld, 2003; Shinwari et al., 2007; Kim et al., 2004; Barbaro et al., 2006; Castellarnau et al., 2007; Dzyadevych et al., 2006).

5. Conclusions

A CMOS neuroelectronic interface integrating two-dimensional OSFET arrays with signal-processing circuitry has been proposed and tested. The die-level, post-CMOS process for fabricating OSFETs is proved to be simple and reliable. By retaining metal wires for interconnection, the CMOS-compatible OSFETs can be easily integrated into a two-dimensional array as well as connected with on-chip circuitry. Electrical measurements further indicate that the OSFETs and on-chip circuitry are robust against the micromachining process or exposure to neural saline. Furthermore, biological experiments demonstrate that the OSFET chip can record neural activity as faithfully as conventional tools, while the noise level should be further improved. On the other hand, neural stimulation can only be achieved by applying voltage pulses to multiple OSFETs simultaneously. A careful experiment indicates increasing the size of the OSFET is necessary. This leads to the debate on the practicality of using the same OSFET for both recording and stimulation, even though the technology has been proved feasible. Experiments with cultured neurons will thus be carried out to examine the necessity of employing separate OSFETs to achieve both satisfactory recording selectivity and effective stimulation.

Based on the experiment results, a large-scale, multi-functional neuroelectronic interface using OSFETs will be developed for in vitro study of general neuronal networks. By incorporating the technology of fabricating CMOS microprobes (Ho et al., 2006), CMOS neural probes using OSFETs will be further developed for in vivo applications. Moreover, the transformation of the OSFET arrays into various field-effect biosensors with on-chip circuitry will also be explored.

Acknowledgements

Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.bios.2008.09.007.

References

Banu, M., Tsividis, Y., 1982. Electronics Letters 18, 678–679.
Barbaro, M., Bonfiglio, A., Raffo, L., Alessandrini, A., Facci, P., Barak, I., 2006. IEEE Electron Device Letters 27 (7), 595–597.
Berdondini, L., Van der Wal, P., Guenat, O., de Rooij, N., Koudelka-Hep, M., Seitz, P., Kaufmann, R., Metzler, P., Blanc, N., Rohr, S., 2005. Biosensors and Bioelectronics 21, 167–174.
Bergveld, P., 2003. Sensors and Actuators, B. Chemical 88 (1), 1–20.
Breckenridge, L., Wilson, R., Connolly, P., Curtis, A., Dow, J., Blackshaw, S., Wilkinson, C., 1995. Journal of Neuroscience Research 42 (2), 266–276.
Castellarnau, M., Zine, N., Bausells, J., Madrid, C., Juarez, A., Samitier, J., Errachid, A., 1995. Physical Review Letters 75 (8), 1670–1674.

Castellarnau, M., Zine, N., Bausells, J., Madrid, C., Juarez, A., Samitier, J., Errachid, A., 2007. Sensors and Actuators, B 120, 615–620.

Claverol-Tinture, E., Cabestany, J., Rosell, X., 2007. IEEE Transactions on Biomedical Engineering 54 (2), 331–335.

Cohen, A., Spira, M., Yitshaik, S., Borghs, G., Shwartzglass, O., Shappir, J., 2004. Biosensors and Bioelectronics 19 (12), 1703–1709.

Dzyadevych, S., Soldatkin, A., El'skaya, A., Martelet, C., Jaffrezic-Renault, N., 2006. Analytica Chimica Acta 568 (1–2), 248–258.

Eversmann, B., Jenkner, M., Hofmann, F., Paulus, C., Brederlow, R., Holzapfl, B., Fromherz, P., Merz, M., Brenner, M., Schreiter, M., Gabl, R., Plehert, K., Steinhauser, M., Eckstein, G., Schmitt-Landsiedel, D., Thewes, R., 2003. IEEE Journal of Solid-State Circuits 38 (12), 2306–2317.

Fromherz, P., 1999. European Biophysics Journal with Biophysics Letters 28 (3), 254–258.

Fromherz, P., Carsten, O., Weis, R., 1993. Physical Review Letters 71 (24), 4079–4082.

Fromherz, P., Offenhausser, A., 1990. Science 252 (5010), 1290–1293.

Furshpan, E., Potter, D., 1959. The Journal of Physiology 145, 289–329.

Giovangrandi, L., Gilchrist, K., Whittington, R., Kovacs, G., 2006. Sensors and Actuators, B 113, 545–554.

Greve, F., Lichtenberg, J., Kirstein, K., Frey, U., Perriard, J., Hierlemann, A., 2007. Journal of Micromechanics and Microengineering 17 (3), 462–471.

He, B., 2005. Neural Engineering, 1st edn. Kluwer Academic, New York.

Heer, F., Hafizovic, S., Franks, W., Blau, A., Ziegler, C., Hierlemann, A., 2006. IEEE Journal of Solid-State Circuits 41 (7), 1620–1629.

Heer, F., Hafizovic, S., Ugniwenko, T., Frey, U., Franks, W., Perriard, E., Perriard, J., Blau, A., Ziegler, C., Hierlemann, A., 2007. Biosensors and Bioelectronics 22 (11), 2546–2553.

Ho, M.H., Chen, H., Tseng, F., Yeh, S., Lu, M., 2006. Journal of Micro Mechanics and Micro Engineering 17, 283–290.

Hutzler, M., Fromherz, P., 2004. European Journal of Neuroscience 19 (8), 2231–2238.

Jenkner, M., Müller, B., Fromherz, P., 2001. Biological Cybernetics 84 (4), 239–249.

Jimbo, Y., Kasai, N., Torimitsu, K., Tateno, T., Robinson, H., 2003. IEEE Transactions on Biomedical Engineering 50 (2), 241–248.

Kim, D., Jeong, Y., Park, H., Shin, J., Choi, P., Lee, J., Lim, G., 2004. Biosensors and Bioelectronics 20 (1), 69–74.

Klemic, K., Klemic, J., Reed, M., Sigworth, F., 2002. Biosensors and Bioelectronics 17, 597–604.

Lambacher, A., Jenkner, M., Merz, M., Eversmann, B., Kaul, R., Hofmann, F., Thewes, R., Fromherz, P., 2004. Applied Physics A: Materials Science and Processing 79 (7), 1607–1611.

Lin, J., Chang, S., Chang, C., Lu, S., Chen, H. S, August 2007. Engineering in Medicine and Biology Society 2007, Proceedings of the 29th Annual International Conference of the IEEE, pp. 2365–2368.

Meyburg, S., Goryll, M., Moers, J., Ingebrandt, S., Bocker-Meffert, S., Luth, H., Offenhausser, A., 2006. Biosensors and Bioelectronics 21, 1037–1044.

Meyburg, S., Stockmann, R., Moers, J., Offenhausser, A., Ingebrandt, S., 2007. Sensors and Actuators, B 128 (1), 208–217.

Morin, F., Takamura, Y., Tamiya, E., 2005. Journal of Bioscience and Bioengineering 100 (2), 131–143.

Morrison, S., Madou, M., Frese, K., 1980. Applied Surface Science 6 (2), 138–148.

Olsson, R., Wise, K., 2005. IEEE Journal of Solid-State Circuits 40 (12), 2796–2804.

Parak, W., George, M., Gaub, H., Böhm, S., Lorke, A., 1999. Sensors and Actuators, B. Chemical 58 (1–3), 497–504.

Patolsky, F., Timko, B., Yu, G., Fang, Y., Greytak, A., Zheng, G., Lieber, C., 2006. Science 313 (5790), 1100–1104.

Rutten, W., 2002. Annual Review of Biomedical Engineering, 407–452.

Shinwari, M., Deen, M., Landheer, D., 2007. Microelectronics Reliability 47, 2025–2057.

Tsai, L., Tseng, S., Yeh, S., 2005. Journal of Computational Physiology A: Neuroethology Sensory Neural and Behavioral Physiology 191, 347–354.

Vassanelli, S., Fromherz, P., 1998. Applied Physics A: Material Science and Processing 63, 459–463.

Vato, A., Bonzano, L., Chiappalone, M., Novellino, A., Tedesco, M.B., Bove, M., Martinoia, S., 2003. First International IEEE EMBS Conference on Neural Engineering, pp. 466–469.

Watanabe, A., Grundfest, H., 1961. Journal of General Physiology 45, 267–308.

Weis, R., Fromherz, P., 1997. Physical Review E 55 (1), 877–889.

Zeck, G., Fromherz, P., 2001. Proceedings of the National Academy of Sciences of the United States of America 98 (18), 10457.

Zigmond, M., et al., 1999. Fundamental Neuroscience. Academic Press, San Diego.