A Resist-Protection-Oxide Transistor With Adaptable Low-Frequency Noise for Stochastic Neuromorphic Computation in VLSI

Tang-Jung Chiu, Ya-Chin King, *Member, IEEE*, Jeng Gong, Yi-Hung Tsai, and Hsin Chen, *Member, IEEE*

***Abstract*—Noise is found to play a beneficial rather than harmful role for neural computation. For example, the sensory neurons exploit stochastic resonance to enhance their sensitivity. This finding has inspired several neuromorphic systems attempting to use noise for computation. Nevertheless, an adaptable noise source is essential for taking the most advantages of noise. This letter presents a resist-protection-oxide (RPO) transistor, which is a defect-rich transistor between the drain implant and the gate. The RPO defects enhance greatly the low-frequency noise of the transistor. The noise level is further adaptable over two decades by the drain voltage. Moreover, the transistor is fully compatible with the standard CMOS logic technology without requiring additional masks or process steps. All the features underpin the development of stochastic neuromorphic computation in integrated circuits.**

***Index Terms*—Defect screening, low-frequency noise, noise adaptability, resist protection oxide (RPO), stochastic computation.**

I. Introduction

LOW-FREQUENCY noise, particularly for the $1/f$ noise, is found to exist naturally in many perspectives, including the composed music [1], the human cognition [2], the DNA sequence [3], and the neural activity [4]. In addition, the noise is further found to play a beneficial rather than harmful role for neural computation [5]–[7]. For example, the sensory neurons are able to exploit the phenomenon called stochastic resonance (SR) to enhance the detection of weak signals [6], [7]. The SR refers to the addition of an optimal level of noise to boost the information content during signal transmission. The SR principle has been adopted to improve the sensitivity of cochlear implants [8], as well as to inspire novel treatments on diabetes and stroke [9]. There are also neuromorphic systems attempting to use noise for computation [10].

All these applications demand adaptable noise sources for optimizing the beneficial role of the noise. For example, an optimal noise level is crucial for the SR [6]–[9]. Instead of relying on circuit techniques to produce pseudorandom signals, the feasibility of using the low-frequency noise of transistors to generate truly random signals has also been proposed in [11] and [12]. However, these methods require extra process steps and simply boost the low-frequency noise to a usable extent without considering the noise adaptability. An octagonal dual-gate transistor is thus proposed in [13], employing an extra gate on the shallow trench isolation (STI) to adapt the extra noise induced by the STI–silicon interface.

This letter presents a resist-protection-oxide (RPO) field-effect transistor (FET) (Fig. 1), which utilizes the defect-rich RPO film to enhance the low-frequency noise. The noise level is adaptable by the drain voltage, based on the principle that the drain-side depletion would be able to screen off the RPO defects [14], analogous to the mechanism explored to achieve the multilevel flash memory [15]. This mechanism allows the RPO-FET to control the noise level directly with a relatively lower voltage than that required by the dual-gate transistor in [13]. In addition, the RPO-FET is fabricated with the standard CMOS 0.18-μm logic technology without additional masks or process steps, facilitating the integration with ordinary CMOS integrated circuits.

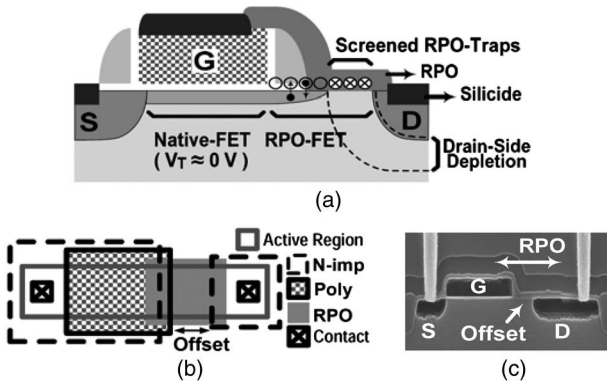

Fig. 1. RPO-FET structure. (a) Cross-sectional view. (b) Layout. (c) SEM image.

II. Device Structure

Fig. 1(a) shows the cross-sectional structure of the RPO-FET, transformed from a native n-channel transistor. The drain implant is shifted away from the edge of the polygate, resulting in an "offset" region over which the RPO film is deposited. Both the native option and the RPO film are available in the standard 0.18-μm CMOS logic process provided by the Taiwan Semiconductor Manufacturing Company (TSMC). The native option

Manuscript received April 19, 2011; revised May 19, 2011; accepted May 25, 2011. Date of publication June 27, 2011; date of current version August 24, 2011. This work was supported by the National Science Council, Taiwan. The review of this letter was arranged by Editor W. S. Wong.

T.-J. Chiu, Y.-C. King, Y.-H. Tsai, and H. Chen are with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan (e-mail: chiu.tang.jung1@gmail.com; ycking@ee.nthu.edu.tw; yhtsai@well.ee.nthu.edu.tw; hchen@ee.nthu.edu.tw).

J. Gong is with the Department of Electrical Engineering, TungHai University, Taichung 40704, Taiwan (e-mail: jgong@thu.edu.tw).

Digital Object Identifier 10.1109/LED.2011.2158384

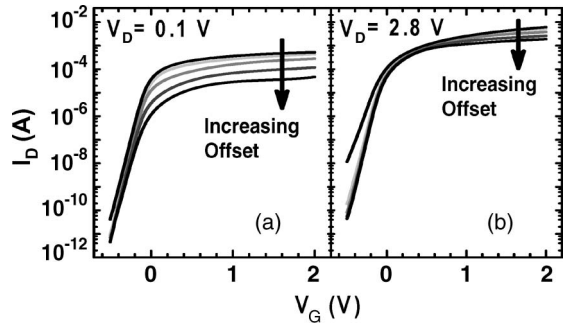

Fig. 2. Measured I_D–V_G curves of the RPO-FETs with different offsets (0, 0.2, 0.3, 0.4, and 0.5 μm) and with $V_S = V_B = 0$ V. (a) $V_D = 0.1$ V. (b) $V_D = 2.8$ V.

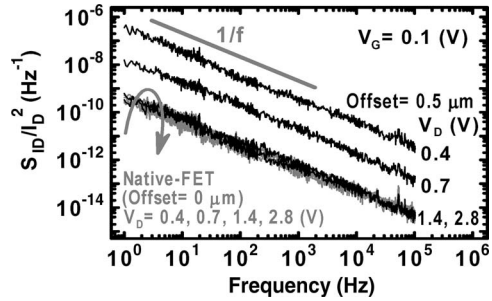

Fig. 3. Influence of V_D on the normalized noise spectra of (black lines) the RPO-FET with a 0.5-μm offset and (gray lines) the native FET, as $V_G = 0.1$ V and $V_S = V_B = 0$ V.

blocks the p-well engineering for the n-channel transistor. The transistor thus has a nearly zero threshold voltage due to low channel-doping concentration. The RPO is a deposited oxide film that is originally used for blocking silicidation. Compared to the thermal oxide, the RPO contains numerous dangling bonds and, thus, interface traps for inducing low-frequency noise [16]. To preserve the p-type channel underneath the RPO, the n-type lightly doped drain (NLDD) implant is further cancelled. As the RPO-FET can only be controlled by the fringing field of the polygate, the channel doping underneath the RPO should be kept low to reduce the threshold voltage of the RPO-FET. This is achieved by both the native option and the cancellation of the P-pocket implant, which shares the same process mask as the NLDD implant.

Fig. 1(a) indicates that the proposed device has a structural feature of two transistors in series. One is the native FET overlapped by the polygate and the gate oxide, and the other is the RPO-FET. The RPO-FET contains much more interface traps, dominating to generate the low-frequency noise. The likelihood for the channel carriers to interact with the RPO traps can be further modulated by the drain-side depletion. As the drain voltage increases, the depletion region can extend horizontally to "screen off" part of the RPO traps [14], [15], so as to reduce the low-frequency noise [17]. Moreover, the low channel doping underneath the RPO enables the depletion region to extend effectively with a low drain voltage, facilitating low-voltage circuit design.

With the layout in Fig. 1(b), the fabricated RPO-FET exhibits the structure revealed by the scanning-electron-microscopy (SEM) image in Fig. 1(c). The offset region of the RPO-FET is clearly visible. To investigate how the offset affects the low-frequency noise, RPO-FETs with 20-μm gate width, 1.2-μm gate length, and different offsets (0, 0.2, 0.3, 0.4, and 0.5 μm) are fabricated for comparison. The zero-offset FET serves as a control experiment for identifying the electrical characteristics contributed solely by the native FET.

III. Results and Discussion

Fig. 2 shows the measured I_D–V_G characteristics of the RPO-FETs with different offsets. All the curves exhibit the typical feature of a transistor transiting from weak to strong inversion as V_G increases. Therefore, the offset region covered by the RPO film acts as a transistor, and all the RPO-FETs enter strong inversion after $V_G > 0$ V. As V_D is small (0.1 V), Fig. 2(a) shows that increasing the offset causes the drain current to reduce. This is because the total channel resistance increases with the offset. As V_D increases to 2.8 V, Fig. 2(b) shows that the I_D–V_G curves of all the RPO-FETs tend to overlap with one another when V_G is low (< 0.5 V). This result indicates that the RPO-FET is nearly screened off by the drain depletion, such that the dc behavior is dominated by the native FET [14]. For $V_G > 0.5$ V, the increased fringe field of the gate counteracts the drain voltage to reduce the drain depletion [14]. As a result, the RPO-FET regains its influence gradually with increasing V_G. Fig. 2(b) also reveals that the zero-offset FET has a worst subthreshold swing, attributed to the channel punch-through effect. This nonideal effect is common for native transistors with low channel doping, while, with the existence of the RPO-FET, the nonideal effect is released because the total channel length increases.

The noise spectra of all transistors are measured with a noise analyzer (BTA 9812B) at the room temperature. Fig. 3 shows the low-frequency noise spectra of both the RPO-FET with a 0.5-μm offset and the zero-offset FET (i.e., the native FET) for comparison. The noise spectra ($S_{\rm ID}$) are normalized with respect to I_D^2 for different drain voltages. For the native FET, V_D has negligible impact on the noise level, agreeing with the ordinary model of the low-frequency noise [18]. Contrarily, the noise level of the RPO-FET with a 0.5-μm offset increases by more than two decades as $V_D = 0.4$ V. This result demonstrates that the RPO-FET can introduce low-frequency noise effectively. In addition, the noise level is adaptable over two decades as V_D changes from 0.4 to 1.4 V. As $V_D > 1.4$ V, the RPO-FET has the same noise level as the native FET. This indicates that the RPO-FET is nearly screened off by the drain depletion, such that only the noise of the native FET remains.

To study how the noise level depends on the offset and the drain voltage, the low-frequency noise spectra of the RPO-FETs at different V_D are further measured. The noise power ratio (NPR) defined in (1) is then calculated. The total noise power (TNP) is first obtained by integrating the noise spectrum over a specific bandwidth (BW) of interests (from 1 Hz to 100 kHz). Dividing the TNP by I_D^2 then gives

$$\text{NPR} = \frac{\text{TNP}}{I_D^2} = \frac{\int_{\rm BW} S_{\rm ID}(f)df}{I_D^2}. \quad (1)$$

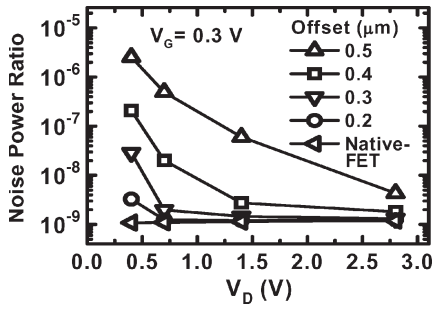

Fig. 4. Dependence of the NPRs on V_D for the RPO-FETs with different offsets as $V_G = 0.3$ V and $V_S = V_B = 0$ V.

Fig. 4 shows the NPRs of the RPO-FETs with different offsets. With $V_G = 0.3$ V and V_D varying from 0.4 to 2.8 V, the larger offset induces the higher NPR due to increased RPO traps. The NPR, i.e., the effect of the RPO traps, can be reduced by either increasing V_D or shortening the offset. The RPO-FETs with an offset greater than 0.2 μm have their NPRs adaptable over two decades. However, the adaptable range for the RPO-FET with an offset of 0.2 μm is relatively small. This is because the lateral diffusion of the drain implant could extend over the offset region and thus mask off the effect of the RPO-FET. Therefore, an offset greater than 0.2 μm is important to ensure the noise enhancement and adaptability of the RPO-FET.

It is notable that, although the noise level of an ordinary transistor also increases with its drain current, the result in Fig. 4 demonstrates that the RPO-FET allows the transistor noise to be enhanced and adapted in a much more power-efficient manner, i.e., with high NPRs. The enhancement comes from the increased traps of the RPO film instead of increased current consumption. Moreover, the higher noise requires a lower drain voltage, which results in even lower power consumption.

IV. Conclusion

An RPO transistor has been formed by placing an RPO film above a drain-shifted transistor with the NLDD and the P-pocket implant cancelled. The RPO layer is proved useful for enhancing the low-frequency noise by more than two decades. Moreover, the noise level is adaptable by the drain voltage, and the required dynamic range of the drain voltage is reasonably low, facilitating circuit design with the RPO-FET. Although the noise characteristics of the RPO-FET can vary from one device to another, the wide adaptable range would facilitate the optimization of the noise level disregarding the process variation. Comparison among the RPO-FETs with different offsets further indicates that a minimum offset is essential for the intriguing noise characteristics to become significant. Based on the promising results, circuits incorporating the RPO-FET will be designed and tested.

Acknowledgment

The authors would like to thank the TSMC for chip fabrication, the High-Frequency Division, National Nano Device Laboratories, for the support on noise measurements, and Prof. C. F. Huang for valuable discussion.

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