

Embedded analogue nonvolatile memory with feedback-controlled programming circuit on-chip

C.C. Lu, P.L. Chen, C.D. Huang and H. Chen

An analogue nonvolatile memory is presented, which is not only CMOS-compatible but also capable of storing analogue currents with a resolution of more than eight bits. The programming process is controlled by a hysteretic comparator on-chip, which stops the injection current automatically by negative feedback, regardless of the programming nonlinearity and device mismatches. With the simple, on-chip programming circuit, the proposed analogue memory is capable of storing currents ranging from 1 to 18 μA accurately with negligible variations across different memory cells.

Introduction: The neuromorphic system in [1] first employed floating-gate devices to store analogue values non-volatily, facilitating analogue computation in parallel and in large scale. An analogue non-volatile memory array for storing audio data was further demonstrated in [2]. While the two pioneering works were based on the customised EEPROM technology, Diorio *et al.* proposed the CMOS-compatible (or *embedded*), analogue nonvolatile memory, extending its application to a wide variety of analogue circuits [3]. However, the accuracy of analogue storage in an array had been limited by the non-linearity of programming mechanisms and device mismatches. One proposed solution was calculating the required drain voltage for a target current, and then programming each memory cell iteratively by short pulses of injection currents [4]. This solution not only required a large, off-chip system to implement the programming algorithm but also relied on precise sensing of the drain current of each memory cell.

This Letter presents an embedded, analogue nonvolatile memory, fabricated with the standard CMOS 0.35 μm technology by the Taiwan Semiconductor Manufacturing Co. With a simple, on-chip programming circuit controlling the programming current by negative feedback, the memory cell is able to store analogue currents with comparable accuracy to that in [4]. The feedback control further eliminates the effect of device mismatches, guaranteeing a negligible variation across different memory cells.

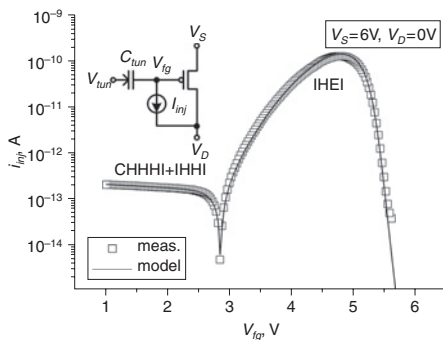


Fig. 1 Measurement and simulation results of injection current against floating gate voltage with $V_S = 6\text{ V}$ and $V_D = 0\text{ V}$

Gate current models: The proposed analogue memory is based on the p -type transistor, the gate of which is isolated and connected with a poly-Nwell capacitor (C_{num}), as illustrated by the inset in Fig. 1. The device structure is analogous to that in [3], while a control gate formed by a second poly layer is not included and the transistor operates in the strong-inversion region instead. In each programming process, electrons in the floating gate are first removed (erased) by Fowler-Nordheim (FN) tunnelling through C_{num} . Hot-electron injection (I_{inj}) is then induced in the p -type transistor to program the floating gate. The white squares in Fig. 1 show the measured I_{inj} against the gate voltage (V_{fg}), averaged over the measurements of five transistors with $W/L = 5\ \mu\text{m}/1\ \mu\text{m}$. As V_{fg} increases from 1 to 6 V, I_{inj} is dominated by hole and electron injections in turn, resulting in a self-convergent point around $V_{fg} = 2.8\text{ V}$. I_{inj} preceding the self-convergent point involves both channel hot-hole injection (CHHI) and impact-ionised hot-hole injection (IHHI), while beyond this point, only impact-ionised hot-

electron injection (IHEI) is involved [5]. According to [6], CHHI in strong inversion can be modelled as (1), with IHHI and IHEI as (2):

$$I_{CHHI} = \alpha_1 I_S (|V_{DS}| - V_{DSAT})^2 e^{\beta_1 / |V_{DS}| - V_{DSAT}} \quad (1)$$

$$I_{IHHI \& IHEI} = \alpha_2 I_S (|V_{DS}| - V_{DSAT})^3 e^{\beta_2 / |V_{DS}| - V_{DSAT}} \quad (2)$$

where I_S represents the channel current, V_{DS} the drain-to-source voltage, and V_{DSAT} the saturation voltage. The process-dependent parameters α_i and β_i are extracted as $\alpha_1 = 6.37 \times 10^{-12}$ and $\beta_1 = 3.6185$ for CHHI, $\alpha_2 = 7.95 \times 10^{-13}$ and $\beta_2 = 6.5716$ for IHHI, and $\alpha_2 = 0.93$ and $\beta_2 = -97.427$ for IHEI. Assuming that CHHI and IHHI occur with equal probability, the total injection current is modelled as $I_{inj} = I_{IHEI} - (I_{CHHI} + I_{IHHI})/2$. The black curve in Fig. 1 shows the simulated I_{inj} , agreeing with the measurement satisfactorily.

Proposed circuit: Fig. 2 shows the proposed analogue memory circuit and its photograph. The four transistors encircled by the dotted line constitute a memory cell, wherein the common gate of M_{fg1} and M_{fg2} is the floating node (V_{fg}). M_{fg1} is the programming transistor, generating hot-electron injection into V_{fg} when M_{inj} turns on. C_C is added to reduce the charge-injection errors induced by the switching of M_{inj} . M_{fg2} is the readout transistor the current of which represents the memorised current and is buffered by M_1 . Compared to the single-transistor cell employed in [3], the proposed architecture has the advantage of avoiding charge injection or hot-carrier injection into V_{fg} during the readout process, as the programming current can be completely switched off by turning off M_{inj} and the drain voltage of M_{fg2} is fixed by V_{bias} through M_1 . In addition, the memorised current is independent of the characteristics of M_{fg1} , which could change or degrade after undergoing injection current for a long term. All the other transistors except for M_{10} and M_{11} form a current comparator to be shared among different memory cells. M_6 – M_9 copy I_{ref} for comparison with the I_{out} copied by M_1 – M_5 . Through the two-stage inverter (M_{i1} – M_{i4}), the comparator controls the turning on of M_{inj} and thus the occurrence of hot-electron injection at M_{fg1} . To improve the comparator precision, M_{h1} – M_{h2} are added to introduce the hysteretic effect with its width controlled by V_{hys} . The programming procedures are as follows: (i) a voltage pulse of 8 V is applied to V_{num} to remove electrons from the floating node, causing I_{out} to be much smaller than 1 μA ; (ii) I_{ref} ranging from 1 to 18 μA is presented. As $I_{ref} > I_{out}$, the current comparator turns on M_{inj} , inducing hot-electron injection to increase I_{out} ; (iii) once I_{out} equals I_{ref} , the comparator turns off M_{inj} and stops the electron injection. The feedback control gives the great advantage of programming I_{out} automatically and accurately, regardless of the programming nonlinearity, mismatches across different memory cells, and the potential degradation of M_{fg1} . In the prototype design, a voltage buffer is also added to monitor the voltage change at V_{fg} .

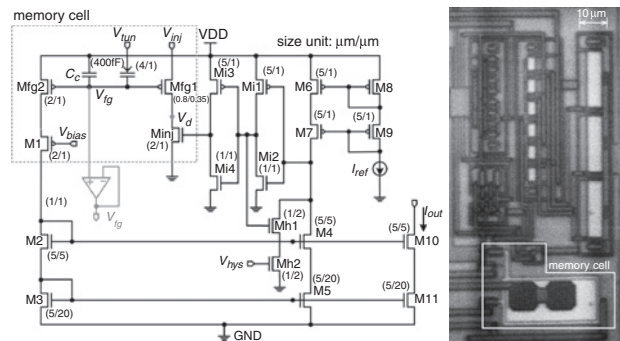


Fig. 2 Full circuit of analogue nonvolatile memory and its chip photo

Measurement results: The inset of Fig. 3 showed the measured dynamics of V_{fg} as the analogue memory was programmed to different current levels. In each experiment, V_{fg} was initialised to around 4.3 V by FN tunnelling, and then programmed at $t = 0\text{ s}$ when I_{ref} was presented. As I_{out} equals I_{ref} , V_{fg} converged into an equilibrium level and stored the target current reliably. The maximum programming time was around 38.3 ms for $I_{ref} = 18\ \mu\text{A}$, shorter than that (350 ms) achieved in [4]. After I_{ref} was removed, I_{out} was measured by a source-meter (Keithley 2602). Within the range $I_{ref} = [1\ \mu\text{A}, 18\ \mu\text{A}]$, the maximum programming error, $\Delta I_{out} = I_{out} - I_{ref}$, was 50 nA, as

shown in Fig. 3. The effective bit resolution was thus calculated as $\log_2(17/0.05)$, yielding a resolution of more than eight bits. Fig. 4 shows the statistics of the measurements over four identical memory cells, revealing clearly the linearity and the precision of the analogue memory. The magnified window shows that the maximum standard deviation of 5.5 nA occurs at $I_{ref} = 6 \mu\text{A}$. Such a small variation is attributed to the feedback control by the comparator, and is of particular importance for an analogue memory array.

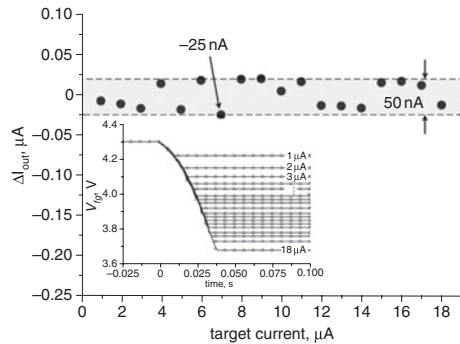


Fig. 3 Measured dynamics of V_{fg} (inset) and precision of proposed analogue memory with its on-chip programming circuit

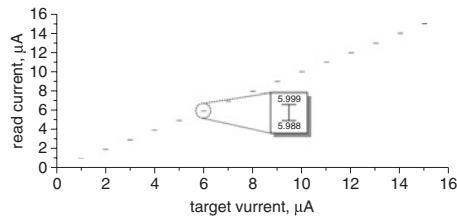


Fig. 4 Statistics over measurement of four analogue memory cells programmed by on-chip, hysteretic comparator

Error bars indicate standard deviations

Conclusions: An embedded, analogue nonvolatile memory with a simple, on-chip programming circuit has been designed and tested.

The measurement results demonstrate that the programming circuit is capable of storing analogue currents into the memory as accurately as the off-chip system in [4], with a shorter programming time and negligible variations across different memory cells. The promising performance mainly comes from the use of a hysteretic comparator to control the programming current automatically by negative feedback. To extend the application of the proposed circuit, a large array of analogue nonvolatile memory will be further developed.

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